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A FAST BINARY TO BCD CONVERSION FOR B/D MULTI-OPERAND ADDER

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Abstract - This paper design a new architecture for a 8 bit Binary to BCD (BD) converter which forms the core of our Proposed high speed high performance and low power decimal Multi-operand Adder. It is intend to design that contains various improvements ended existing architectures. These include an improved BD Converter that helps in reducing the delay reducing area of the Multi-operand decimal Adder. Simulation results indicate that with a insignificant reduce in area, the proposed BD converter reveals an improvement of more than 75 % in power over earlier designs. Further the decimal Multi-operand Adder realize faster design .

Key Words - Carry Save Adder, BCD, Ripple Carry Adder.

I. INTRODUCTION

The utilize of decimal arithmetic has been increasing day by day over binary due to Increase in the applications of internet banking and many applications there are many others places where precision and accuracy is very Important part . Binary digits have a disadvantage of not being able to represent digits like 0.1 or 0.7, requires an infinitely frequent binary number. The availability of multi-operand decimal adders can facilitate financial and commercial applications and internet based on existing huge databases system. The simultaneous addition of several decimal numbers is the common operation in multiplication and division algorithms. Multi-operand addition is a vital operation as it is a core component of arithmetic operations, such as division and multiplication. In case of decimal multiplication Multioperand decimal addition comes in handy for quickly summing large amounts of decimal data. This design introduces a multi-operand decimal addition algorithm by employing high speed binary to BCD converter circuit, which speeds up the process of decimal addition. A new design for binary to BCD converter circuit is proposed. Further, analysis is done with respect to the existing binary to BCD converter architectures. The proposed algorithm is fundamentally unlike from multi-operand BCD addition algorithms [3, 5] since conciliator BCD corrections are not done rather correction is done at the final stage to get proper BCD results. As the decimal corrections are achieved separately from the calculation of the binary sum, such that the layout of the binary carry-save adder does not require any further rearrangement, the design can perform as unified Binary/ BCD multi-operand adder. In the next section, we present preliminary information about the previous work on multi-operand adders and discuss the binary to BCD converter.

II. CARRY SELECT ADDER

In Present generation in VLSI system, are more focused in the reduction of area , power and delay with increasing the speed of operation of the circuit. Particularly a carry select adder is a way to implement an adder , which ia a logic element that can computes the (n+1) bit sum of two n bit numbers. The carry select adder is simple but rather fast, having a gate level depth of o(√n) . The carry select adder generally consists of two ripple carry adders and a multiplexer Circuitry. Adding two n-bit numbers with a carry-select adder is done with two ripple carry adder . One time with supposition of carry input as 0 and another time with carry consider as 1.After the results are calculated, the final sum and the final carry is selected is selected with the multiplexer by the earlier produce carry out. The speed in the SQRT CSLA is dependent on the carry generation of the previous cascaded RCA. The sum of the each bit is generated successively one after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many electronic applications to alleviate the problem of carry circulation delay by independently generating the multiple carries and then select the carry to generate the sum. conversely, the CSLA is not area efficient since it contains multiple Paris of cascaded RCA with input Cin=0 and Cin=1, to generate partial sum and carry, then the final sum and carry are selected by multiplexers.

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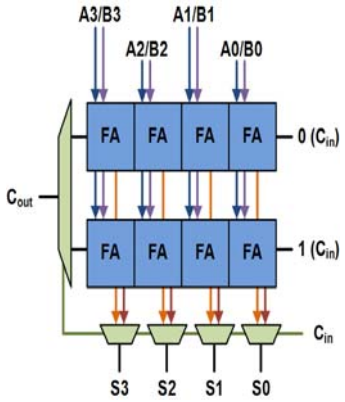

Fig.1 Carry select adder

III. CARRY SAVE ADDER

Carry save adder is also a type of digital adder,which is used in computer microarchitecture to compute the sum of three or more n-bit numbers in binary.It differs from other digital adder since it has outputs of two numbers of same dimension as the inputs,one which is a sequence of partial sum bits and another which is a sequence of carry bit.

It is desired in many cases to add more than two numbers together.The simplest way of adding m numbers all together is to add the first two,then add that sum to the next,and so on.This contains m-1 additions for a total gate delay.The reduction in delay can be a result of using carry save adder.A carry-save adder is just a set of one bit full adders,without any carry chaining.therefore , an m-bit CSA receives three m-bit operands and generates two m-bit values.The most important application of carry save addr is to calculate the partial products in integer multiplication.This allows for arcitectures , where a tree of carry - save adders is used to calculate the partial products very fast.One normal adder is then used to add the last set of carry bits to the last partial products to give the final multiplication results.usually a very fast carry-look ahead or carry select adder is used for this last stage in order to obtain the optimal performance.

Fig.2 Carry save adder

IV. PROPOSED WORK

A carry-select adder is segregate into categories , each of which – except for the LSB – performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. Generally a four bit carry select adder generally consists of two ripple carry adders and a multiplexer circuitry The conversion of the achieve sum from the carry select adder is given into the shift and add three converter, using which we can attain a BCD value.

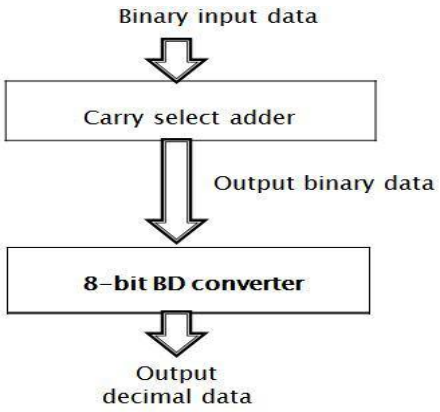

Fig. 3 Design block diagram

V. BCD CONVERTER

In the proposed binary to decimal converter for conversion process we are using shift and add 3 algorithm.

Steps Used In Algorithm

- Shift the binary number left one bit. If 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column.
- If the binary value in any of the BCD columns is 5 or greater, add 3 to that value in that BCD column.
- Repeat the above process.

VI. RTL VIEW OF CIRCUIT

RTL view of binary to bcd converter consist of three inputs clk ,rst,and binary _in shown in fig. 4

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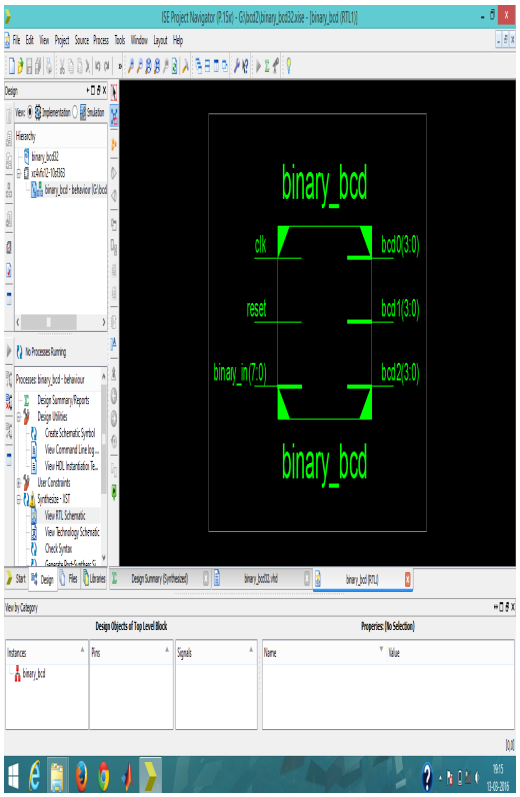

Fig.4 RTL view of binary to bcd converter

Transistor level architecture of binary to bcd converter show look up table for binary to bcd converter shown in fig. 5

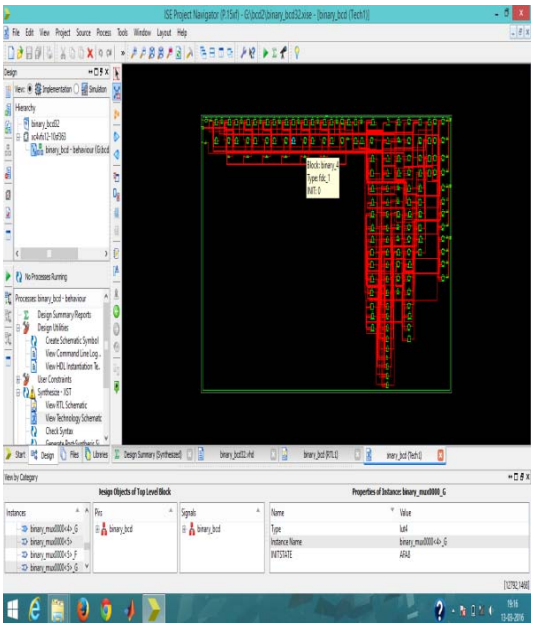

Fig.5 RTL view of binary to bcd converter

Top view module of binary to bcd converter shown in fig .6

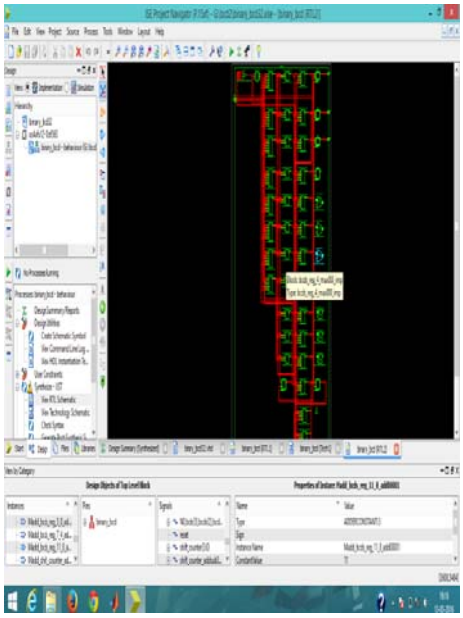

Fig.6 RTL view of binary to bcd converter

VII. SIMULATION RESULT

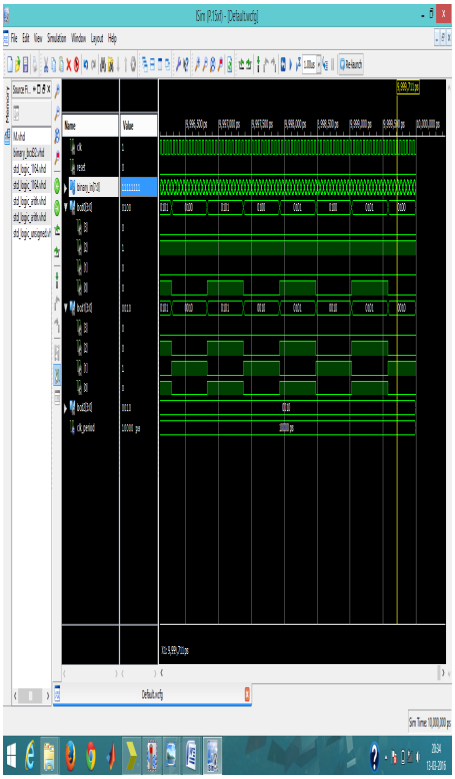

Fig. 7 simulation result of design

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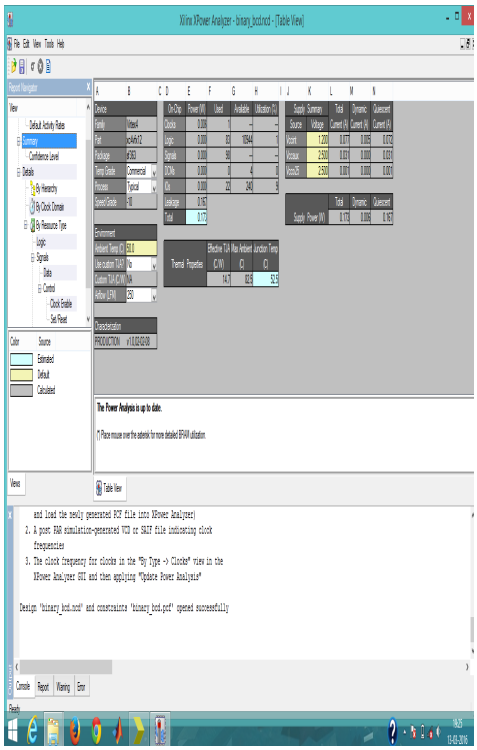
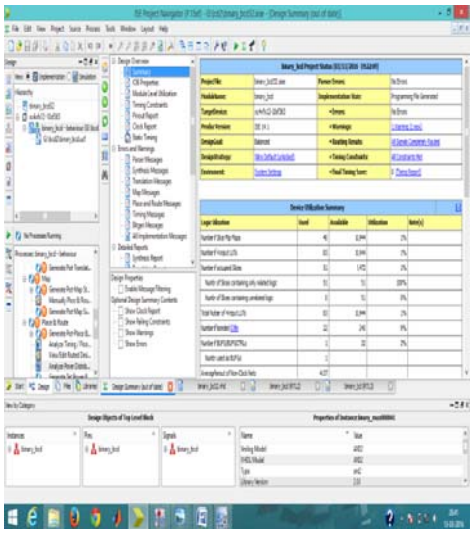


Fig. 8 show power window

Summary OF binary to bcd design which is show look up table of different I/O



VIII. CONCLUSION

In this proposed approach, which consist of a carry save adder and binary to BCD converter gets a better result compared to the existing design and simulation results shows the delay and area variations which is a key advantage. In the proposed system the delay is decreased to 75 % when compared to existing design.

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The research on "**Fast Binary To BCD Conversion For B/D Multi-Operand Adder**" is made possible through the help and support from everyone nearby me. The topic given to me is a part of my stream in 2-years of my master degree (M.Tech). I have tried my best to present this information as clearly as possible by using basic terms and I hope it will be comprehended by the widest spectrum of researchers, analysts , and students for further studies. I have completed this study under the guidance of prof. **Hari Shanker Srivastava.** It's my immense pleasure to acknowledge his esteemed scholarly guidance, assistance, and knowledge.

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