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A Literature Review on Various Topologies used in Multilevel Voltage Source Inverters

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Abstract- **This paper presents a brief study of some most common multilevel inverter topologies and control techniques. The advantages of multilevel inverter topologies such as such as low power dissipation on power switches, lower harmonic distortion and electromagnetic interference generation are made it a preferable choice for the application in medium and high power systems. However the quality of output power also depends upon the applied switching technique to control the inverter and is responsible for producing the required output while maintaining the harmonic distortion at the lowest possible value. Besides the presentation of some standard models this paper also reveals some important aspects of these models. Finally the preferences for selection of topology and control techniques according to various requirements and constrains are presented in tabular form which can be used as basis for selecting the optimal inverter topology according applications requirements.**

Keywords- Multilevel Voltage Source Inverter (MVSI),

I. INTRODUCTION

The properties of multilevel inverters such as lower common mode voltage, lower across the switches voltage, lower voltage variation ratio and reduced harmonic contents inoutput voltage and current, encouraged the designer to adopt the multilevel inverters(MLI) for the applicability in the areas of medium voltage and high power systems.

MLI topologies are broadly classified into three types 1) diode clamped MLI(DC-MLI), 2) flying capacitor MLI (FC-MLI), 3) Reversing Voltage Multilevel Inverter (RVMLI) and 4) cascaded multi-cell inverter. However the hybrid and asymmetric hybrid inverter topologies are also developed according to the combination of existing MLI topologies or applying different DC bus levels respectively. The basic topologies of MLIs are presented in Figure 1.1. Recently the applications area of MLIs includes induction machine and motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission systems(FACTS), and static compensators. In motor drive applications the diode clamped inverters, especially the three-level structure, is widely adopted and preferred over other multilevel inverter topologies. However, the increasing complexity with number of clamping

Diodes for the DC-MLIs, limits its application for the higher level inverters.

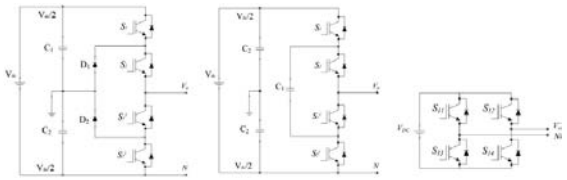

Fig. 1.1- Different MLI topologies, DC-MLI (left), FC-MLI (center) and HB-MLI (right)

Comparing similarity with DC-MLI the FC-MLIs uses balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. The FC-MLI topology requires$(m-1)*(m-2)/$ 2balancing capacitors per phase for an m-level inverter which multiplicatively increases with the levels of inverter topologies. DC-link balancing is another limiting factor for such topologies. The solution for the high complexity DC-MLI and FC-MLIs topology is achieved by H-Bridge MLI

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(CHB-MLI) which requires minimum number of components for a given number of levels. The structure of cascade multilevel inverters contains a series of H-bridge blocks to produce the required output from a number of DC sources. The properties of cascaded multilevel inverters discussed so far makes it perfect choice for using various pulse width modulation control strategies to accurately control it. In addition to these topologies, several modulation and control techniques have been developed for multilevel inverters including selective harmonic elimination PWM (SHE-PWM),sinusoidal PWM (SPWM), space vector PWM (SVM), and similar variations of the three main algorithms. Furthermore the modulation methods of MLIs classified according to switching frequencies as seen in Figure 1.2.

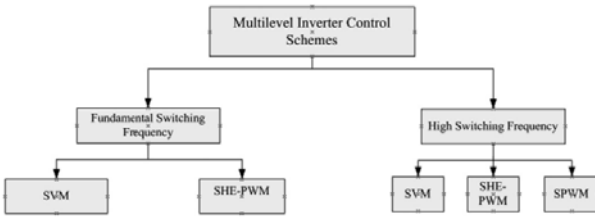

Fig.1.2- MLI control techniques classification structure.

The SPWM control method is very popular in industrial applications owing to its harmonic reducing opportunities by using several phase shifting options on carrier signal. In the SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Several multicarrier techniques have been developed to reduce the THD ratios, based on the classical SPWM with triangular carriers. Another alternative modulation technique is SVM strategy, which has been used appropriately in three-level inverters. The SVM and SHE-PWM methods are fundamental frequency switching methods and perform one or two commutations of the power semiconductors during one cycle of the output voltages to generate a staircase waveform.

Rest of the paper presents different topologies of multilevel inverters, the existing control methods for MLIs and applications, based on the available literatures, finally the tabular comparison of different aspects are also performed.

II. THE CONCEPT OF MULTILEVEL INVERTERS

The two-level inverters is the simplest form of multilevel inverters and can be used to explain the basic working principle of multilevel inverters as seen in Figure 1.3. Presently most of the multilevel inverters uses a DC voltage source to generate AC output. Since the two-level inverters has only two levels hence can only create two different output voltages of amplitudes $V_{dc}/2$ and $V_{dc}/2$across the load, where the V_{dc} represents the voltage of DC source.

To produce an AC output firstly the provided DC voltage source is divided into two appearing different voltage sources which are then alternatively switched by using PWM, see Figure 1.3.

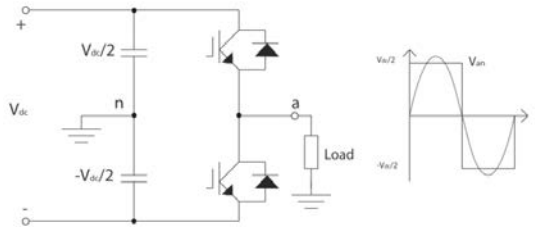

Fig.1.3- two-level inverter topology (left), waveform (right)

Although this method is quite simple and effective for producing AC but it does induces harmonic distortions in the output voltage, with Electromagnetic Interference and high dv/dt(when compared to multilevel inverters). This may cause a serious problems for the applications which require low distortion AC voltage (such as sophisticated electronically controlled Systems).

To reduce the harmonic distortion the concept of Multilevel Inverters (MLI) is utilized which produces multiple discrete levels to closely match the output waveform with sinusoidal AC signal. These discrete voltage levels are generated by adding/ subtracting the available levels with each other's (Figure 1.4).

Although the higher number of voltage levels in the inverter produces much smoother waveform, but this also makes the design more complicated, as it requires more components and a much complicated controller technique.

The creation of multilevel output voltage from the combination of input can be understood by the functionality of three level inverters as shown in Figure 1.4.

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It is called a three-level inverter because everyphase-leg can produce three discrete voltages$V_{dc}/2$, $0, -V_{dc}/2$, as shown in first part of Figure 1.3.

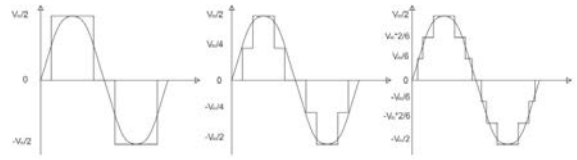

Fig.1.4- A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency.

The basic difference between the two-level and three-level inverter design is that the required number of switched exceeds in each phase-leg to double, with two additional clamping diodes connected between neutral (voltage divider capacitors midpoint) and the upper and lower switches. For generating the required waveform a proper switching operation is repeatedly performed. The extension to the higher level could be achieve by adding switch pairs, clamping diodes and capacitors similar to done in extending the two level to three level are required see Figure 1.5, the result is a multilevel inverter with clamping diode topology.

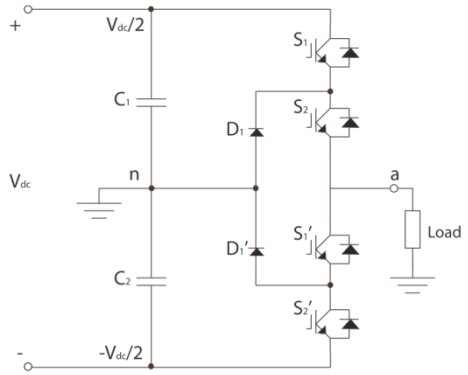

Fig. 1.5- One phase leg of a three-level inverter

III. TOPOLOGIES OF MULTILEVEL INVERTERS

Presently a number of topologies are available for the multilevel inverters which are adapted according to the application specific requirements.

This section presents some of the most widely used topologies:

1. Neutral-Point Clamped Multilevel Inverter (NPCMLI) also known as Diode Clamped Multilevel Inverter.
2. Capacitor Clamped Multilevel Inverter (CCMLI) also known as Flying Capacitor Inverter.
3. Reversing Voltage Multilevel Inverter (RVMLI), also known as H-Bridge MLI.
4. Cascaded Multi-cell Inverter, CMCI

3.1 Neutral-Point Clamped Multilevel Inverter

(NPCMLI) also known as Diode Clamped Multilevel Inverter: The NPCMLI topology uses the voltage clamping diodes. It firstly creates a common DC-bus with different voltage levels which derived by dividing the input voltage by an even numbers of serially connected capacitors acting as voltage divider. The number of capacitors depends on the voltage levels in the inverter Figure 1.6. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to $m-1$ number of switches pairs, where m is the numberof voltage levels in the inverter (voltage levels it can generate).

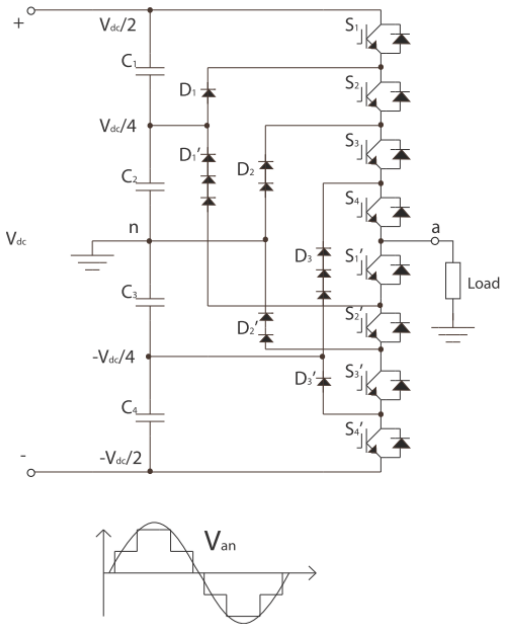

Fig.1.6- One phase-leg for a five-level NPC Inverter

The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. For example, in Figure 1.6 all diodes are rated for $V_{dc}/4$ ($V_{dc}/(m-1\ in\ general)$ and the D_1' diode need to block $3V_{dc}/4$and therefore there are three diodes

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in series. However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find.

3.2 Capacitor Clamped Multilevel Inverter (CCMLI) also known as Flying Capacitor Inverter: it is similar to the NPCMLI topology except it uses Capacitor Clamped (CC), or Flying Capacitor (to hold the voltages to the desired values) instead of Clamping Diode, another difference is the capacitor are used to provide the output voltage and connected to two switches in opposite sides with no midpoint connection, which can be seen in Figure 1.7. As for the NPCMLI, m − 1 number of capacitors on a shared DC-bus, where m is the level number of the inverter, and 2(m−1) switch-diode pairs are used.

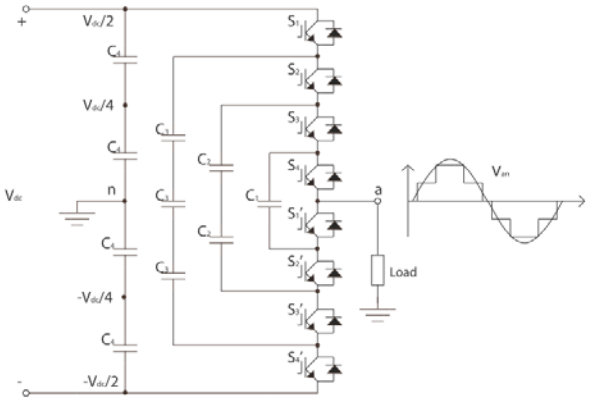

Fig.1.7- A Capacitor Clamped Multilevel Inverter with five voltage levels.

The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages the number of switching combinations increases.

3.3 Reversing Voltage Multilevel Inverter (RVMLI), also known as H-Bridge MLI: this is the most recently proposed topology (was proposed during late 2008), Figure 1.8, the main advantage of this topology over the more popular MLI topologies, the NPCMLI and CCMLI, is it needed lesser number of components when components with equal ratings are used however the number of components increases, as components with different ratings are used.

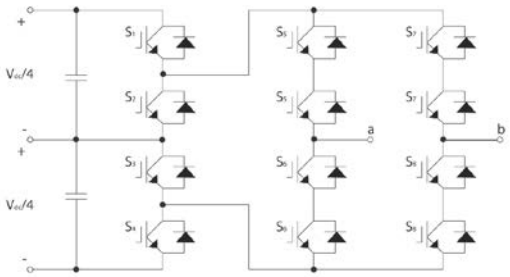

Fig.1.8- One phase-leg for a five-level Reversing Voltage Multilevel Inverter

Two advantages with the RVMLI are simpler controlling, since the modulation is divided in two parts (positive half-wave and reversing) and that it does not have a voltage unbalance problem if separate sources are used. It is however true for several topologies that separate sources can solve the voltage unbalance problem. As for the CMCI the RVMLI is capable of putting out the full range of its DC-side voltage, dividing the need for the DC-side voltage by two for the same output voltage compared to other topologies, such as the NPCMLI

3.4 Cascaded Multi-cell Inverter, CMCI: A Cascaded Multi-cell Inverter (CMCI) differs in several ways from NPCMLI and CCML Iin how to achieve the multilevel voltage waveform. It uses cascaded full-bridge inverters with separate DC-sources, in a modular setup, to create the stepped waveform. In Figure 1.9 one phase-leg of a five-level Cascaded Multi-cell Inverter is shown. Each full-bridge can be seen as a module and it is only these modules that build up the CMCI topology. One full-bridge module is in itself a three-level CMCI, and every module added in cascade to that extends the inverter with two voltage levels. In Figure 1.9 there are two full-bridge modules creating the five different voltage levels available. Applications suitable for the CMCI are for example where photovoltaic cells, battery cells or fuel cells are used.

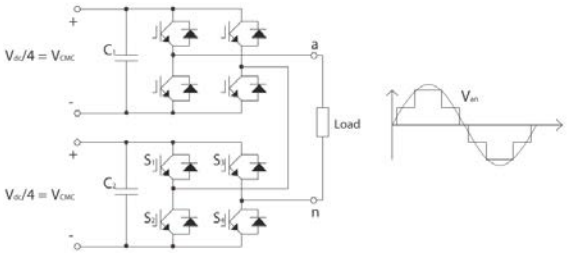

Fig. 1.9- A five-level Cascaded Multi-cell Inverter

Such an example could be an Electric Vehicle there several power cells exists. The sources in each full-

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bridge need to be isolated if the inverter is going to be implemented in an active power transfer application, for voltage balance reasons since there is no common DC-bus to recharge the sources energy content. However, since the CMCI uses separate energy sources it is well suitable for renewable energy or energy/fuel cell applications there every separate voltage source could be isolated. A drawback for the energy/fuel cell applications is however that the sources must be charged individually or through the inverter. The CMCI requires fewer components, every voltage level requires the same amount of components. However, the number of sources are higher, for the phase-leg to be able to create a number of m voltage level s =(m – 1)/2sources are required.

Table 3.1- Comparison of Different Multilevel Inverter Topologies

Comparison Criteria	Topology			
	NPCMLI	CCMLI	RVMLI	CMCI
Number of Components	$(m-1)*(m-2)$	$(m-1)*(m-2)$	3*(m−1)	(m – 1)/2
Voltage Balancing Problem	An additional balancing circuit required or more complex control methods can be implemented.	The unequal workload cause voltage unbalance but by using the redundant switching states the unbalances can be controlled	For several topologies that separate sources can solve the voltage unbalance problem.	The sources must be charged individually or through the inverter to overcome voltage unbalance problem
Output Voltage Span	$-V_{dc}/2\ to\ V_{dc}/2$	$-V_{dc}/2\ to\ V_{dc}/2$	$-V_{dc}\ to\ V_{dc}$	$-V_{dc}\ to\ V_{dc}$
Switching Table Size	Medium	Large	Small	Medium
Controlling	Normal	Complex	Easy	Normal
Advantages	1. All of the phases share a common dc bus, which minimizes the capacitance requirements. 2. The capacitors can be pre-charged as a group. 3. Efficiency is high for fundamental frequency switching.	1. Phase redundancies are available for balancing the voltage levels of the capacitors. 2. Real and reactive power flow can be controlled. 3. The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.	1. The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1). 2. The series of H-bridges makes for modularized layout and packaging. 3. This will enable the manufacturing process to be done more quickly and cheaply.	1. Suitable for renewable energy or energy/fuel cell applications there every separate voltage source could be isolated. 2. Capable of putting out the total voltage source magnitude in both positive and negative direction. 3. Requires fewer components, every voltage level requires the same amount of components.

Disadvantage	1. Real power flow is difficult. 2. The number of clamping diodes required is quadratically related to the number of levels.	1. Control is complicated to track the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same voltage level and startup are complex. 2. Switching utilization and efficiency are poor for real power transmission. 3. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters.	1. Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.	2. The sources in each full-bridge need to be isolated if the inverter is going to be implemented in an active power transfer application. 3. A drawback for the energy/fuel cell applications is however that the sources must be charged individually or through the inverter

IV. CONCLUSION

Based on the available literature on conventional multilevel inverter topologies general and special characteristic, application areas, advantages and disadvantages has been presented. The outcome of the work shows that there is no single solution available and hence needed separate topology for different applications however many new hybrid topologies can be designed using the combinations of three main MLI topologies and one may found an optimal solution for a group of applications.

V. REFERENCES

[1] IlhamiColak, ErsanKabalci, RamazanBayindir "Review of multilevel voltage source inverter topologies and control schemes", Energy Conversion and ManagementVolume 52, Issue 2, February 2011, Pages 1114–1128.

[2] Andreas Nordvall "Multilevel Inverter Topology Survey", Department of Energy and Environment Division of Electric Power Engineering,Chalmers University of Technology,Göteborg, Sweden, 2011.

[3] Hirofumi Akagi "Classification, Terminology, and Application of theModular Multilevel Cascade Converter (MMCC)", IEEE Transactions on Power Electronics, Vol. 26, No. 11, November 2011.

[4] Alessandro LuizBatschauer, Samir Ahmad Mussa, Marcelo Lobo Heldwein, "Three-Phase Hybrid Multilevel Inverter Basedon Half-Bridge Modules", IEEE Transactions on Industrial Electronics, Vol. 59, No. 2, February 2012.

[5] JakobGlasdam, JesperHjerrild, Łukasz Hubert Kocewiak, Claus LethBak "Review on Multi-Level Voltage Source Converter Based HVDC Technologies for Grid Connection of Large Offshore Wind Farms", Power System Technology (POWERCON), 2012 IEEE International Conference, Oct. 30 2012-Nov. 2 2012.

[6]SurinKhomfoi and Leon M. Tolbert "Multilevel Power Converters", University of Tennessee.

[7] Dr. Keith Corzine "Operation and Design of Multilevel Inverters", University of Missouri – Rolla.

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