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An Efficient Topology and Control Strategy for Multilevel Voltage Source Inverters

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Abstract: Application of multilevel converters because of its superior performance gaining the popularity in industrial applications. As mentioned the superior performance which largely influenced by the high quality output waveform of multilevel converters in comparison to two-level inverters. In this paper, firstly a multilevel converter topology with efficient placement of switches for increasing the voltage levels in the output waveform is presented and then an efficient low complexity minimal component digital control block is developed to control the converter. The presented multilevel converter requires minimum number of switching and controlling devices. Particular attention has been given to the control circuitry to obtain optimal control of the waveform with minimum number of gates and other logical devices to make it suitable for FPGA/CPLD implementation. Finally the presented multilevel converter with proposed control circuitry is analyzed for different operating conditions; the quality assessments in terms of total harmonic distortionis also performed to evaluate the performance of the proposed multilevel inverter.

Keywords- Multilevel Inverters, Digital Control, Inverter Topologies.

I. INTRODUCTION

Multilevel converters include a series of switches, and DC voltage sources, the output waveforms of which is created by cascading the DC sources is specific patterns. Compared to a two-level voltage source inverter (VSI), multilevel VSI enables to synthesize the output voltages with higher numbers of levels or with lower harmonic distortion and electromagnetic interference. By increasing the number of levels in the output waveform multilevel inverters output voltages are more close to sinusoidal waveform, which reduces the harmonic distortion, however, a greater number of levels increase the number of devices and complexity of the control, furthermore the increasing the number of devices reduces the overall reliability and efficiency of the inverter. One most common solution of this problem is using the inverters with lower number of levels and then apply an LC output filter to limit the distortion but it requires bulky components and imposes the operational complexity.

Presently many literatures have been already published to improve the performance of multilevel converters, some of them dealt with new topologies such as hybrid multilevel converter, optimization of components and asymmetric multilevel converter to improve the output voltage waveform quality while others presented the advanced control strategies such as artificial intelligence, fuzzy logic etc..Although both direction of research provides many good solutions but still the limitations of each technique cannot be fully avoided, for such conditions a combine approach can provide much better solution by complementing the limitations each other's. This paper presents a multilevel converter topology which uses reduced number of switches to obtain the much higher levels in output waveform with low complexity digital control system. The rest of the paper is arranged as follows, the second section presents a brief review of some recent and related literatures, followed by a brief explanation of multilevel inverters. The fourth section the proposed approach is presented followed by the performance analysis calculations in fifth section followed by the simulation results in sixth section. Finally seventh section presents the conclusion derived on the basis of simulation results.

International Research Journal of Engineering & Applied Sciences
www.irjeas.com, ISSN(o): 2322-0821, Volume 3, Issue 1, January 2015 – March 2015, Page 01-06

II. LITERATURE REVIEW

This section presents a brief review of some recently published literatures on the multilevel inverters. The three-phase asymmetrical cascaded multilevel voltage source inverter with series connected power cells in asymmetrical configuration to cancel redundant output levels and maximize the number of levels in output waveform generated by the inverter [1]. The design considerably reduces the number of utilized switches, insulated gate driver circuits, voltage standing on switches, installation area and cost, to further improve the quality a high-frequency pulse-width modulation (PWM) control method is employed. Saad Mekhilef et al [3] is presented a Vector Control Method for Three-Stage Hybrid Cascaded Multilevel Inverter, the proposed algorithm avoid the undesirable high switching frequency for high and medium voltage stages while the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage states. Switching algorithms of the high and medium voltage stages have been also developed to assure fundamental switching frequency operation. The low-voltage stage is controlled using SVM to achieve the reference voltage vector exactly and to set the order of dominant harmonics as desired. Half-Bridge Modules based Hybrid Multilevel Inverter is presented in [4], the model employs a conventional three-phase voltage source inverter (VSI) linking series connected half-bridge modules at each phase. With the proposed connection, a large portion of energy can be processed by the VSI by employing a single multi-pulse rectifier, while smaller power shares are processed within the half-bridge modules. Thus, reduces the requirements for insulated dc sources. A new topology for sub-multilevel inverter is proposed in [7] and then extended with serially connected sub-multilevel inverters as a generalized multilevel inverter. The presented multilevel inverter uses reduced number of switching devices. Special attention has been paid to obtain optimal structures regarding different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources, etc. The FPGA as a control circuit for generation of the digital pulse width modulation (DPWM) signal for the single-phase cascaded H-bridge multilevel inverter is proposed by Akbar Ahmad et al [9], the FPGA chip hardware implementation produces accurate results even at a high computational speed. Hirofumi Akagi et al [10] presented a detailed and useful literature on Classification, Terminology, and Application of theModular Multilevel Cascade Converter (MMCC). Single DC Source based Asymmetric Cascaded Multilevel Inverters is proposed by Javier Pereda et al [11], since the CHB (Cascaded H-bridge) and ACHB (Asymmetric Cascaded H-bridge) inverters require a large number of bidirectional and isolated dc supplies that must be balanced, and as any multilevel inverter, they reduce the power quality with the voltage amplitude. They presented a solution to improve the already mentioned drawbacks of ACHB inverters by using a high-frequency link using only one dc power source. This single power source can be selected according to the application (regenerative, non-regenerative, and with variable or permanent voltage amplitude).

III. MULTILEVEL INVERTERS

The two-level inverters is the simplest form of multilevel inverters and can be used to explain the basic working principle of multilevel inverters as seen in Figure 3.1. Presently most of the multilevel inverters uses a DC voltage source to generate AC output. Since the two-level invertershas only two levels hence can only create two different output voltages of amplitudes $V_{dc}/2$ and $V_{dc}/2$ across the load, where the V_{dc} represents the voltage of DC source.

To produce an AC output firstly the provided DC voltage source is divided into two appearing different voltage sources which are then alternatively switched by using PWM, see Figure 3.

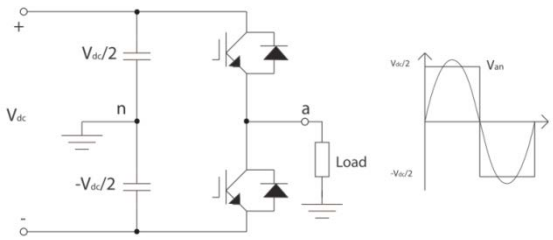

Fig.3.1 - Two-level inverter topology (left), waveform (right)

Although this method is quite simple and effective for producing AC but it does induces harmonic distortions in the output voltage, with Electromagnetic Interference and high dv/dt (when compared to multilevel inverters). This may cause a serious problem for the applications which require low distortion AC voltage (such as sophisticated electronically controlled Systems).
Toreduce the harmonic distortion the concept of Multilevel Inverters (MLI) is utilized which produces multiple discrete levels to closely match the output waveform with sinusoidal AC signal. These discrete voltage levels are generated by adding/ subtracting the available levels with each other (Figure 4.1).

International Research Journal of Engineering & Applied Sciences
www.irjeas.com, ISSN(o): 2322-0821, Volume 3, Issue 1, January 2015 – March 2015, Page 01-06

Although the higher number of voltage levels in the inverter produces much smoother waveform, but this also makes the design more complicated, as it requires more components and a much complicated controller technique.

The creation of multilevel output voltage from the combination of input can be understood by the functionality of three level inverters as shown in Figure 4.1.

It is called a three-level inverter because every phase-leg can produce three discrete voltages$V_{dc}/2\ ,0,-V_{dc}/2$, as shown in first part of Figure 3.3.

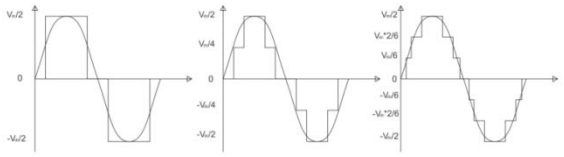

Fig.3.2- A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency.

The basic difference between the two-level and three-level inverter design is that the required number of switched exceeds in each phase-leg to double, with two additional clamping diodes connected between neutral (voltage divider capacitors midpoint) and the upper and lower switches. For generating the required waveform a proper switching operation is repeatedly performed. The extension to the higher level could be achieve by adding switch pairs, clamping diodes and capacitors similar to done in extending the two level to three level are required see Figure 4.2, the result is a multilevel inverter with clamping diode topology.

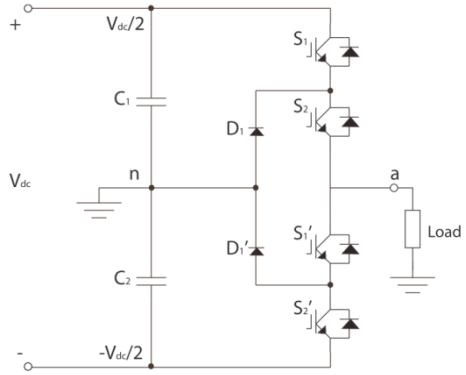

Fig.3.4- One phase leg of a three-level inverter

IV. PROPOSED APPROACH

The proposed system utilizes only four IGBT switches to generate the 9 different levels of output voltage for one full waveform. The circuit uses separate H-Bridge as polarity inverter, the advantage of using separate H-bridge is to reduce the component counts while using multiple units for higher levels of output.

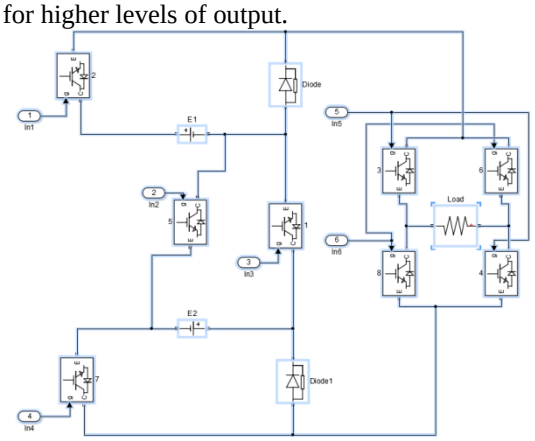

Fig.4.1- Topology of the Proposed System

Different voltage levels are generated by the achieving configurations (as shown in figures 4.2 to 4.5) by properly operating the switches. In some figures the diode blocks are eliminated because in that particular it operating in reverse biased mode.

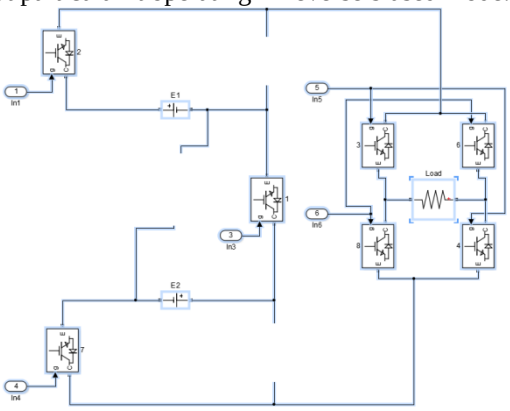

Fig.4.2- Showing the operating condition for output voltage = E1 + E2, the three inputs 1, 3 and 4 are required to held in state '1'.

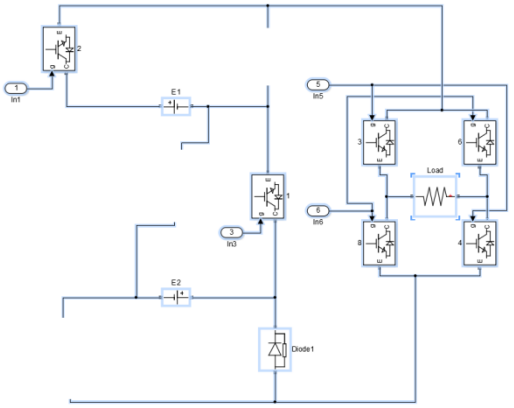

Fig.4.3- Showing the operating condition for output voltage = E1, only two inputs 1 and 3 are required to held in state '1'.

International Research Journal of Engineering & Applied Sciences
www.irjeas.com, ISSN(o): 2322-0821, Volume 3, Issue 1, January 2015 – March 2015, Page 01-06

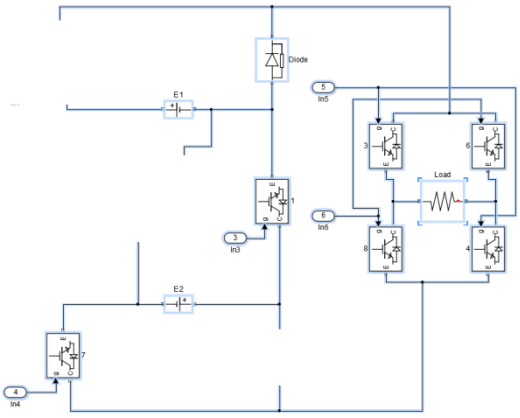

Fig.4.4- Showing the operating condition for output voltage = E2, only two inputs 3 and 4 are required to held in state '1'.

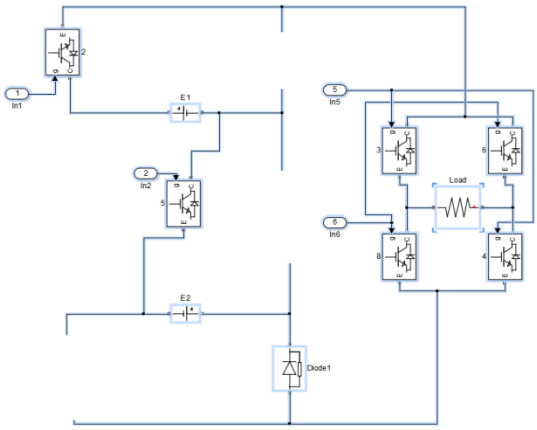

Fig.4.5- Showing the operating condition for output voltage = E1 - E2, only two inputs 1 and 2 are required to held in state 1'.

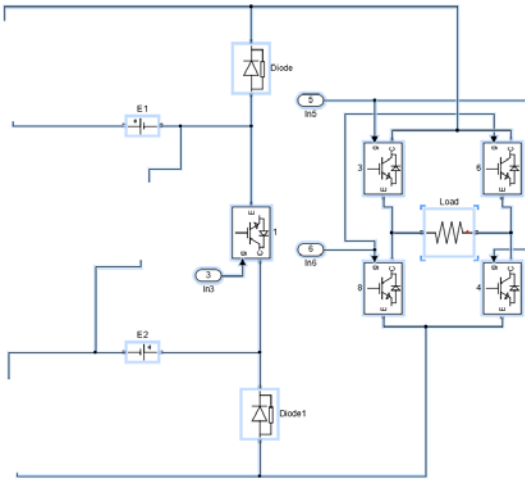

Fig.4.6- Showing the operating condition for output voltage = 0, only two inputs 1 is required to held in state '1'.

Table 4.1- Switches States for obtaining Different Levels

Output Voltage	Control Signals for Switches					
	S1	S2	S3	S4	S5	S6
E1+E2	1	0	1	1	1	0
E1	1	0	1	0	1	0
E1-E2	1	1	0	0	1	0
E2	0	0	1	1	0	0
0	0	0	1	0	X	X
-E2	0	0	1	1	0	1
-(E1-E2)	1	1	0	0	0	1
-E1	1	0	1	0	0	1
-(E1+E2)	1	0	1	1	0	1

Now looking to table 4.1, its clear the S5 and S6 are complementary hence the number of inputs can be reduced to 5 because the S6 can be generated by just inverting the S5.

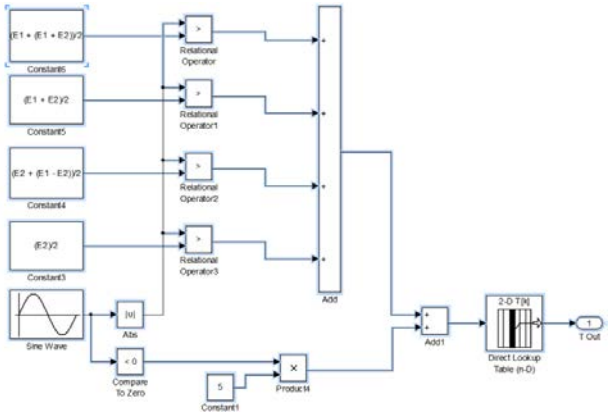

Fig.4.7- Circuit Diagram of the controller (amplitude of the sine wave is E1 + E2). The Table 4.1 data is stored in Lookup Table.

V. SIMULATION RESULTS

The simulation of the proposed model is simulated in MATLAB/SIMULINK environment. To test the applicability of the system it is simulated for resistive and RL loads and the received waveform and their analysis are presented in this section.

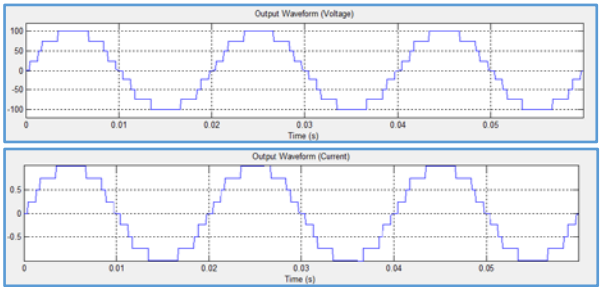

Fig.5.1- Output Voltage and Current Waveforms of inverter with resistive load. E1 = 75Volts and E2 = 25Volts, Load = 100 ohms.

International Research Journal of Engineering & Applied Sciences
www.irjeas.com, ISSN(o): 2322-0821, Volume 3, Issue 1, January 2015 – March 2015, Page 01-06

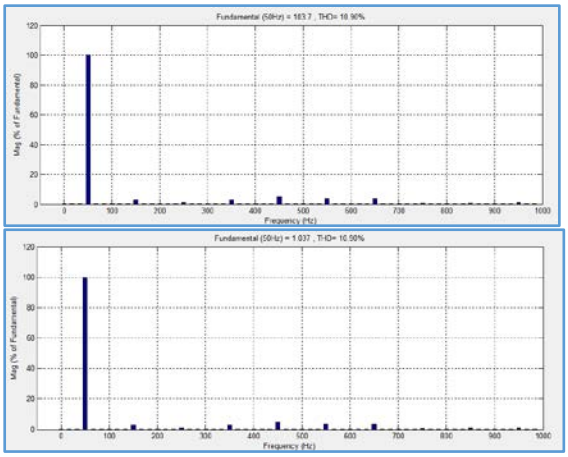

Fig.5.2- Harmonic Components of the figure 10 waveforms.

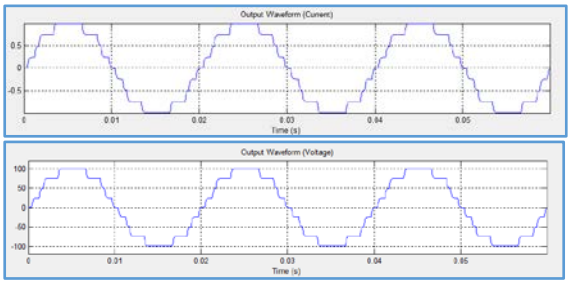

Fig.5.3- Output Voltage and Current Waveforms of inverter with resistive load. E1 = 75Volts and E2 = 25Volts, Load R = 100 ohms, L = 10mH.

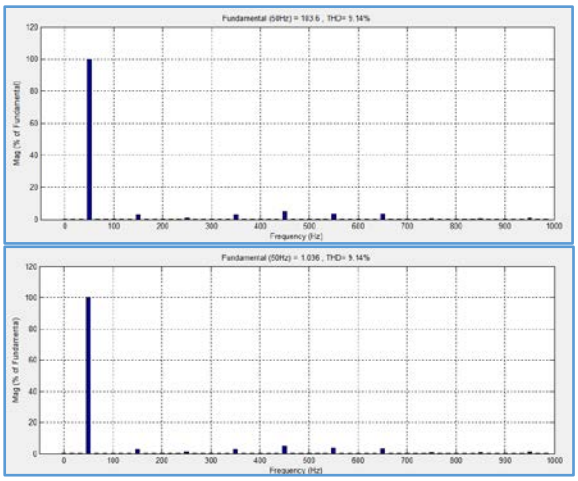

Fig.5.4- Harmonic Components of the figure 5.3 waveforms.

VI. CONCLUSION

An efficient multilevel inverter topology with simple control strategy is proposed in this paper the proposed topology provides every combination of the sources obtainable with minimum active components, also the components used in the proposed controlling system can be easily implemented on FPGA/CPLD which provides it reliability and flexibility. Finally the performed simulation shows that the presented model works properly in different load conditions.

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